

Serial No. 09/878,677

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By Naemi Chapa
(Signature)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : HSIEH, Jeff
Serial No. : 09/878,677
Filed : 6/11/2001
Atty. Docket : PHN 17,803
Group Art Unit : 2615
Examiner : TRAN, Nhan T.
Conf. No. : 2022

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED
CLAIM FOR PRIORITY**

Sir:

This Petition is submitted concurrently with the filing of a Request for Continued Examination (RCE) in response to a Final Office Action mailed March 15, 2006. In accordance with 35 USC 365(a) and 35 USC 119(b)(2), Applicant petitions to accept an unintentionally delayed claim for priority to International Application No. PCT/EP00/11652 filed on November 23, 2000, and published as WO 01/42902 A1 on June 14, 2001. The first page of the

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international publication is enclosed the convenience of the Office.

The International Application on the subject invention was filed on November 23, 2000.

This U.S. Application for the same subject invention was filed June 11, 2001, less than 12 months from the filing date of the International Application.

The Commissioner is authorized to charge any fees under 37 CFR 1.17 associated with this petition to Deposit Account No. 14-1270.

Respectfully submitted,

By 

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914-333-9602

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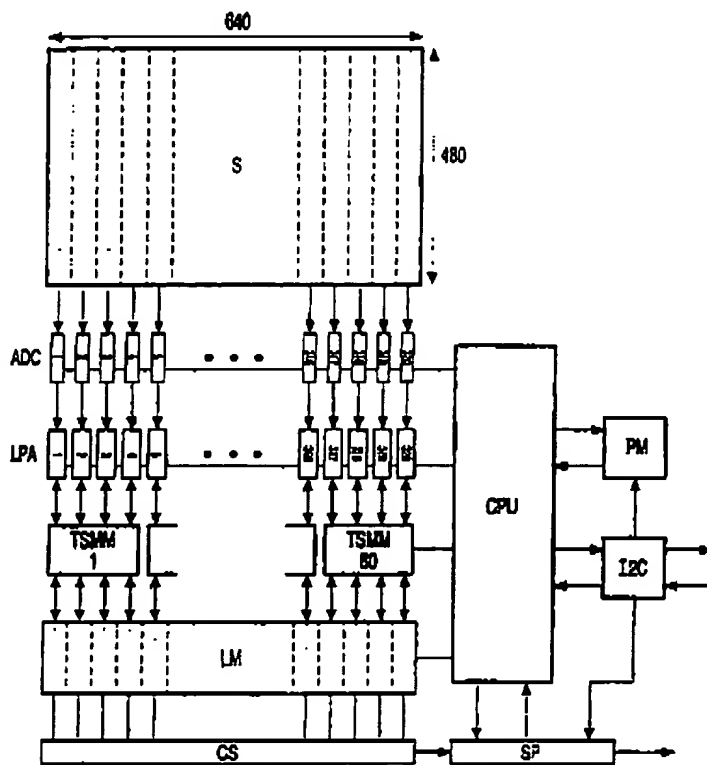
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 For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PARALLEL DATA PROCESSING AND SHUFFLING



(57) Abstract: The invention provides a parallel data processing device having an array of parallel processing elements (LPA1...320) for processing a signal to obtain parallel streams of data, and means (TSM1...80) for shuffling the parallel streams of data in a block-wise manner. The data shuffling means (TSM1...80) have an array of addressable switch memory matrices (TSM1...80) which are each coupled to a predetermined number of processing elements (LPA1...320). The array of switch memory matrices (TSM1...80) solves data flow limitations of highly parallel linear array processors as well as intermediate storage requirements of image processing algorithms. In a camera system the parallel data processing device is combined with a sensor array (S).

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